METHOD AND APPARATUS TO REMOTELY SENSE THE TEMPERATURE OF A POWER SEMICONDUCTOR

CROSS REFERENCE TO RELATED APPLICATIONS

The present invention claims the benefit and priority of U.S. Provisional Application S.N. 60/470,063 (IR-1852 PROV (2-2287)) filed May 12, 2003 and U.S. Provisional Application S.N. 60/477,420 (IR-1852 PROV II (2-3558)) filed June 10, 2003, both entitled "IMPROVED METHOD TO REMOTELY SENSE THE TEMPERATURE OF A POWER SEMICONDUCTOR IN PARTICULAR OF A POWER MOS DEVICE" and further claims the benefit and priority of U.S. Provisional Application S.N. 60/470,476 (IR-1851 PROV (2-2286)), filed May 14, 2003, entitled "CURRENT SENSING DRIVER OPERABLE IN LINEAR AND SATURATED REGIONS", the disclosures of each of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to methods and apparatus to remotely sense the temperature of a power semiconductor device and, in particular, of a power MOSFET device.

In order to prevent damage to power semiconductor devices, the maximum operating temperature of the devices should not be exceeded. It is accordingly important to monitor the temperature of power semiconductor devices so that they can be shut down or the current limited through them if the maximum operating temperature is to reached in order to prevent damages to the devices. The present invention relates to a method and apparatus for remotely and indirectly determining

the temperature of the power semiconductor device, in particular, a power MOSFET by sensing the ON drain-source resistance, i.e., R_{DSON} and thus the voltage between drain and source of the power MOSFET device.

SUMMARY OF THE INVENTION

The above and other objects of the invention are achieved by CLAIM 1

The above and other objects of the invention are also achieved by apparatus for indirectly sensing the temperature of a power MOS device comprising a power MOS device having a current sensing circuit for sensing the current in the power MOS device, a voltage divider coupled between the drain and source of the power MOS device; a comparator coupled to receive at a first input an output of the voltage divider and at a second input a voltage related to the current in the power MOS device, the comparator generating an overtemperature protection signal when a predetermined inequality between the voltages at the first and second inputs to the comparator occurs.

The objects of the invention are further achieved by an apparatus for indirectly sensing the temperature of a power MOS device comprising a power MOS device having a current sense circuit for sensing the current in the power MOS device wherein the current sense circuit includes a circuit for providing a voltage related to the current in the power MOS device from the sensed current, a comparator coupled to receive at a first input a first voltage related to the voltage across the drain and source of the power MOS device and at a second input the voltage related to the current in the power MOS device, the comparator generating an overtemperature protection signal when a predetermined inequality between the voltages at the first and second inputs to the comparator occurs.

The objects of the invention are also achieved by a method for indirectly sensing the temperature of a power MOS device comprising sensing a first voltage

related to the drain-source voltage of the power MOS device, sensing a second voltage related to the current in the power MOS device, comparing the first and second voltages; and generating an overtemperature protection signal when a predetermined inequality between the first and second voltages occurs.

Preferably, the power MOS device has a main current cell and current sense cell, the current sense cell functioning as or as a part of the current sensing circuit..

Other objects and features of the invention will become apparent from the detailed description which follows.

BRIEF DESCRIPTION OF THE DRAWING(S)

The invention will now be described in the following detailed description with reference to the drawings in which:

Fig. 1 shows a first circuit for remotely determining the temperature of a power semiconductor device, in particular, a power MOSFET;

Fig. 1A shows a graph of V_{DS} versus current for various operating temperatures of a power MOS device;

Fig. 1B shows a graph of R_{DSON} versus temperature;

Fig. 2 is a second embodiment of the circuit for remotely determining the temperature of a power MOS device; and

Fig. 2A is a graph explaining the operation of the circuit of Fig. 2.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

With reference now to the drawings, Fig. 1 shows a first embodiment of a circuit for remotely and indirectly determining the temperature of a power MOS device. The power MOS device is generally indicated at 10 and includes a main drain-source cell 10A and a current sense drain-source cell 10B. For example, the current through cell 10A may be 10,000 times the current through cell 10B.

The source of power MOS device main cell 10A is connected to a load 20, which load may have its other terminal grounded. The current sense cell 10B has its source coupled to the drain of a first P channel MOS transistor 15 which may comprise a MOSFET which is coupled in series with a resistor R_{DG} to ground. Resistor R_{DG} is optional and may be provided if the current is to be monitored. Otherwise, the source of transistor 15 is connected to ground. A further P channel MOS transistor, e.g., MOSFET 17, is coupled such that its gate is connected to the gate of transistor 15 and such that its drain is connected to the drain of transistor 10. Its source is connected to a current mirror comprising transistors 30 and 40, connected in a well known current mirror arrangement. The drain of transistor 40 is coupled through resistor R to the drain of transistor 10. The voltage across resistor R is proportional to I_R, which is proportional to the current I_{SEN} in the current sense cell 10B.

An amplifier 19 is coupled such that its non-inverting input is coupled to the source of transistor cell 10B and its inverting input is coupled to the source of cell 10A. A further amplifier 50, operating as a comparator, is coupled as shown and will be described below.

The resistor RDG is external to the integrated circuit of which the MOSFET 10, the transistors 15 and 17, amplifiers 19 and 50 and the current mirror 30,40 are preferably internal components.

MOSFET 40 has its drain coupled in series with the resistor R back to voltage VDD. The comparator 50 is coupled as shown. The comparator 50 has its non-inverting terminal coupled to the common connection between resistor R and the drain of MOSFET 40. The current I_R through transistor 40 determines the current I_R through resistor R, and thus the voltage drop across resistor R. The inverting terminal of comparator 50 is coupled to the source of power MOSFET cell 10A, and thus a voltage related to V_{DS} is present at the inverting terminal.

The circuit of Fig. 1 operates as follows. As the temperature of MOSFET 10 increases, the drain-source voltage also increases. This is shown in the graph of Fig. 1A which shows that V_{DS} increases with current as well as temperature. The maximum temperature of operation for the device shown is 160°C. Above 160°C, the graph is shown cross-hatched because this is an area of operation in which the device may be damaged. Accordingly, it is desired to maintain the operation of device 10 at a temperature below 160°C.

With reference to Fig. 1B which shows in exemplary fashion how R_{DSON} increases with temperature, if the load current is assumed to be constant, then V_{DS} of cell 10A equals R_{DSON} (T°) x IDS, with reference to Fig. 1, where IDS is the drain-source current of cell 10A.

Since R_{DSON} increases with temperature, as shown in Fig. 1B, and since I_R equals the current mirror (30,40) ratio multiplied by I_S which equals the current mirror ratio multiplied by the MOSFET (15,17) ratio multiplied by ILOAD which is equal to a constant because both the mirror ratio of the current mirror 30,40 and the MOSFET ratio between transistors 15 and 17 as well as ILOAD are constants, therefore VR, the voltage across resistor R, is substantially constant. There will thus be a temperature above which V_{DS} is greater than VR. When V_{DS} exceeds VR, the voltage at the inverting input of comparator 50 will drop below the voltage at the non-inverting input, and the operational amplifier 50 will be triggered to output the OTP signal, thus indicating that an overtemperature condition exists.

At a different current level, the trigger temperature is substantially identical since V_{DS} and VR are both proportional to the load current.

In Fig. 1, amplifier 19 sinks the current IS from the current sense cell 10B so that the potential at the source of cell 10B equals the potential at the source of cell 10A. This is because this is a closed loop system and the voltage between the inputs of amplifier 19 are driven to be equal. In this case, IS equals ILOAD times the ratio

of (MOSFET sense/main MOSFET area). A current proportional to IS, in the illustrated example, IS/20 due to the action of transistors 15 and 17, is provided to the current mirror comprising transistors 30 and 40 and thus as current IR through resistor R. A voltage proportional to the current in the current mirror transistor 40 is generated across resistor R and compared via amplifier 50 to VDS. If VDS is greater than VR, the OTP signal is generated.

The circuit of Fig. 1 requires a current mirror and is more complex than the circuit now to be described with reference to Fig. 2. The circuit of Fig. 2 also uses less circuit area when made into an integrated circuit.

Additionally, the circuit of Fig. 1 requires a negative supply to sink current IS. This is difficult to implement in a low side configuration. Further, power dissipation is lower in the circuit of Fig. 2 because the circuit of Fig. 1 requires IS to be sinked ($P = IS \times (V_{DD} - V_{RDG})$).

Fig. 2 shows a second embodiment which uses a simpler circuit. The power MOSFET 10 includes main cell 10A and sense cell 10B. Sense cell 10B is coupled to a resistor RT to a common point with the source of cell 10A. This source connection is coupled to a load 20 in the manner shown. A comparator 50' has one input coupled to the source terminal of the sense cell 10B and the other input coupled to the output of a resistor voltage divider. In particular, the inverting terminal is coupled to the source terminal of the sense cell 10B. The non-inverting terminal of comparator 50' is coupled across the resistor voltage divider coupled between drain and source comprising resistors R1 and R2. In addition, a short circuit current comparator 70 may be provided coupled across resistor RT.

The circuit operates as follows. If the load current is assumed to be constant, and RT to be a low value resistor so that the voltage across it is small, $I_{RT} \approx$ ILOAD/ratio (area of power MOSFET/area of sense cell). This is approximately constant because of the small resistance value. It is acutally not a constant, but

compared to voltage V_{DS}, it is substantially constant. R1 and R2 operate as a voltage divider to provide a voltage at node A proportional to V_{DS}. This is shown in Fig. 2A. The voltage at node A is equal to V_{DS} times R2/(R1 + R2). The voltage at node B is equal to the voltage across the resistor RT which will be small and approximately constant. As the voltage V_{DS} increases with temperature in proportion to R_{DSON} as shown in Fig. 1B, the voltage at node A will become larger than the voltage at node B and the OTP signal will be generated by comparator 50' when the temperature exceeds a present level, here shown as 160°C.

In addition, comparator 70 provides a short circuit current detection signal in the event the current through resistor RT and accordingly the voltage across it exceeds a preset level determined by V_{REF}.

Fig. 2A shows the operation of the circuit of Fig. 2. As shown, line A represents the voltage at the output of the voltage divider R1 and R2. Voltage B represents the voltage across resistor RT which is approximately a constant. As the temperature increases, the voltage A increases above voltage B and the comparator generates the signal OTP.

Although the circuits according to the invention are shown as discrete devices and/or components, the various component are preferably packaged in an integrated circuit, and the components may be made in a way well known to those of skill in the art. For example, the various comparators shown may be developed in known ways from conventional electronic building blocks used in the IC art for making comparator circuits.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Therefore, the present invention should be limited not by the specific disclosure herein, but only by the appended claims.